AN1386
APPLICATION NOTE

Using the DSM2180F3 with the Analog Devices ADSP-2185

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The DSM2180F3 is a system memory device for use with Digital Signal Processors from the popular Analog Devices ADSP-218X family. DSM means Digital signal processor System Memory. A DSM device brings In-System Programmable (ISP) Flash memory, programmable logic, and additional I/O to DSP systems. The result is a simple and flexible two-chip solution for DSP designs. DSM devices provide the flexibility of Flash memory and smart JTAG programming techniques for both manufacturing and the field. On-chip integrated memory decode logic and memory paging logic make it easy to add large amounts of external Flash memory to the ADSP-218X family for bootloading and/or overlay memory. The DSP accesses this Flash memory using either its Byte DMA (BDMA) interface or as external data overlay memory (no DMA setup overhead).

JTAG In-System Programming (ISP) reduces development time, simplifies manufacturing flow, and lowers the cost of field upgrades. The JTAG ISP interface eliminates the need for sockets and pre-programmed memory and logic devices. For manufacturing, end products may be assembled with a blank DSM device soldered to the circuit board and programmed quickly.

In addition to ISP Flash memory, DSM devices add programmable logic (PLD) and up to 16 configurable I/O pins to the DSP system. The state of each I/O pin can be driven by DSP software or PLD logic. PLD and I/O configuration are programmable by JTAG ISP, just like the Flash memory. The PLD consists of more than 3000 gates and has 16 macro cell registers. Common uses for the PLD include chip selects for external devices, state-machines, simple shifters and counters, keypad and control panel interfaces, clock dividers, handshake delay, and muxes. This eliminates the need for small external PLDs and logic devices. Configuration of PLD, I/O, and Flash memory mapping are easily entered in a point-and-click environment using the software development tool, PSDsoft Express™. This software is available at no charge from http://www.psdst.com/html/softcenter2.html.

The two-chip combination of a DSP and a DSM device is ideal for systems that have limitations on physical size and power consumption concerns. DSM memory and logic are “zero-power,” meaning they automatically go to standby between memory accesses or logic input changes, producing low active and standby current consumption.

PURPOSE

The DSM2180F3 device is designed to interface directly with the popular Analog Devices ADSP-218X series of DSPs. The DSM2180F3 device provides bootloading capability and enables the core DSP design to be done with two chips.

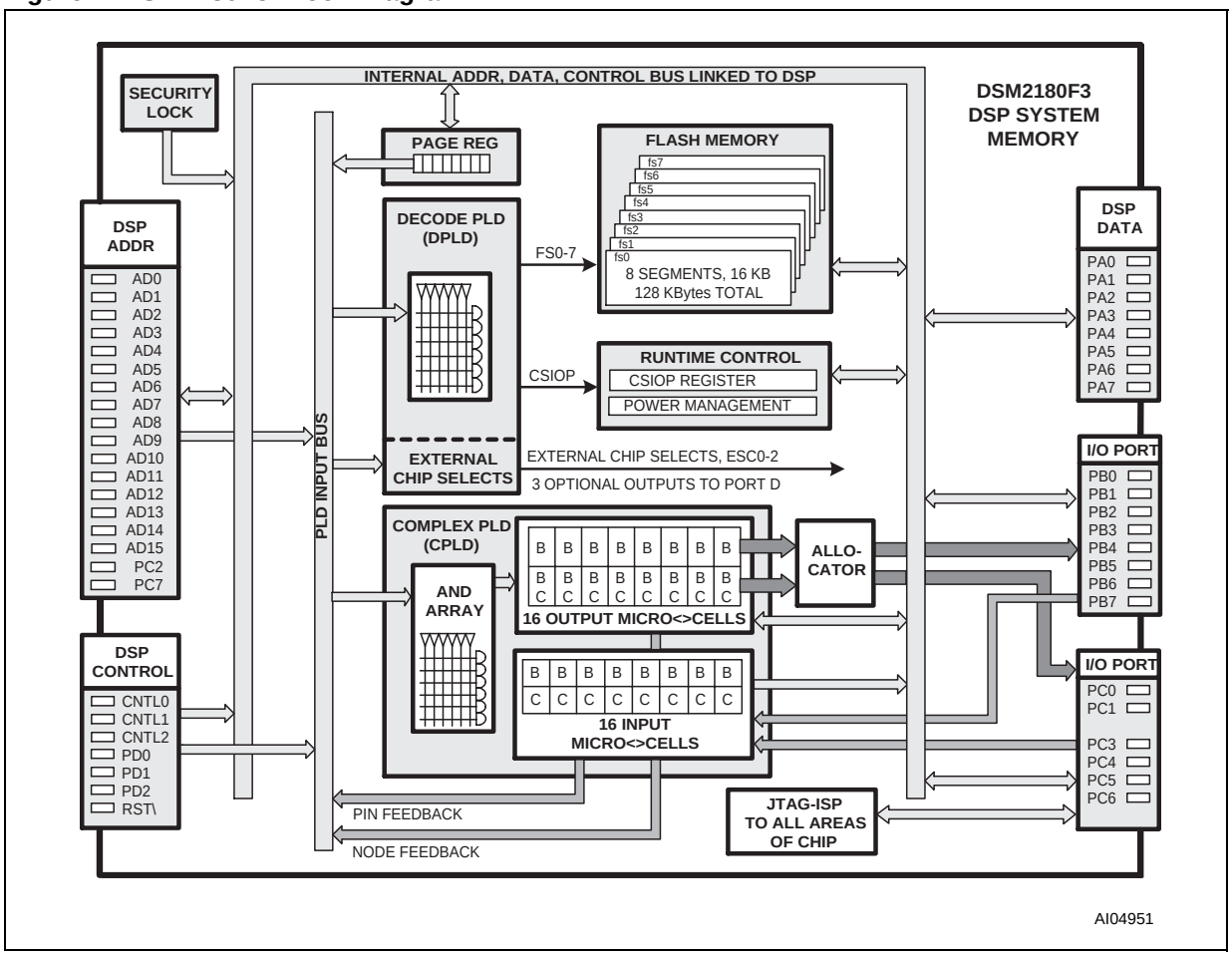
The DSM JTAG port allows In-System Programming (ISP) of a completely blank DSM2180F3 device soldered to the board with no involvement of the DSP, which is ideal for first time programming during manufacturing. Subsequent field updates can also be done via this interface.

This application note addresses the ease of interfacing the DSM2180F3 with the ADSP-2185 DSP. Familiarity with the DSM2180F3 is assumed. Please see the DSM2180F3 data sheet for a detailed description of the device.

DSM2180F3 ARCHITECTURE

Figure 1 is a block diagram of the DSM2180F3.

Figure 1. DSM2180F3 Block Diagram



On-chip features supply the key elements to implement a two-chip DSP System. Flash DSM features include:

- Glueless connection to DSP: easily add memory, logic, and I/O to DSP.

- 128 KBytes of main Flash memory, divided into eight equal individually protected sectors.
- Flash-based PLD with 16 Output Macrocells and 16 Input Macrocells.
- General Purpose PLD that is configurable for external chip-selects or combinatorial logic.
- 19 individually configurable I/O Port pins. Each may be defined as DSP I/Os, PLD I/Os, latched DSP address outputs, or special function I/Os.
- 8-bit Page Register to expand the external address space and implement memory swapping.
- JTAG compliant serial port for true In-System Programming (ISP) of blank devices and reprogramming of devices in the factory or field.

DEVELOPMENT SYSTEMS

This application note provides general guidelines for connecting the DSM2180F3 to the ADSP-218X DSP. In addition, ST provides a specific development kit implementation called the DK-2180 that highlights many of the features of the DSM and ADSP. For more information, see our development kit section of our website: http://www.psdst.com/html/tools.html.

PSDsoft Express is a software development tool that runs on Windows platforms for DSM family development. This tool allows you to configure the DSM using a simple point-and-click interface. DSP bootloader firmware is imported and merged to create a single programming data file (.obj) to program into the DSM. The generated programming data file is then used to program the DSM using one of ST's programmers (PSDpro or FlashLINK) or a 3rd party programmer. For more information on PSDsoft Express, visit http://www.psdst.com/html/softcenter2.html. To see a list of compatible 3rd party programmers, visit http://www.psdst.com/html/psdprog.html.

INTERFACING THE DSM2180F3 WITH THE ADSP-2185

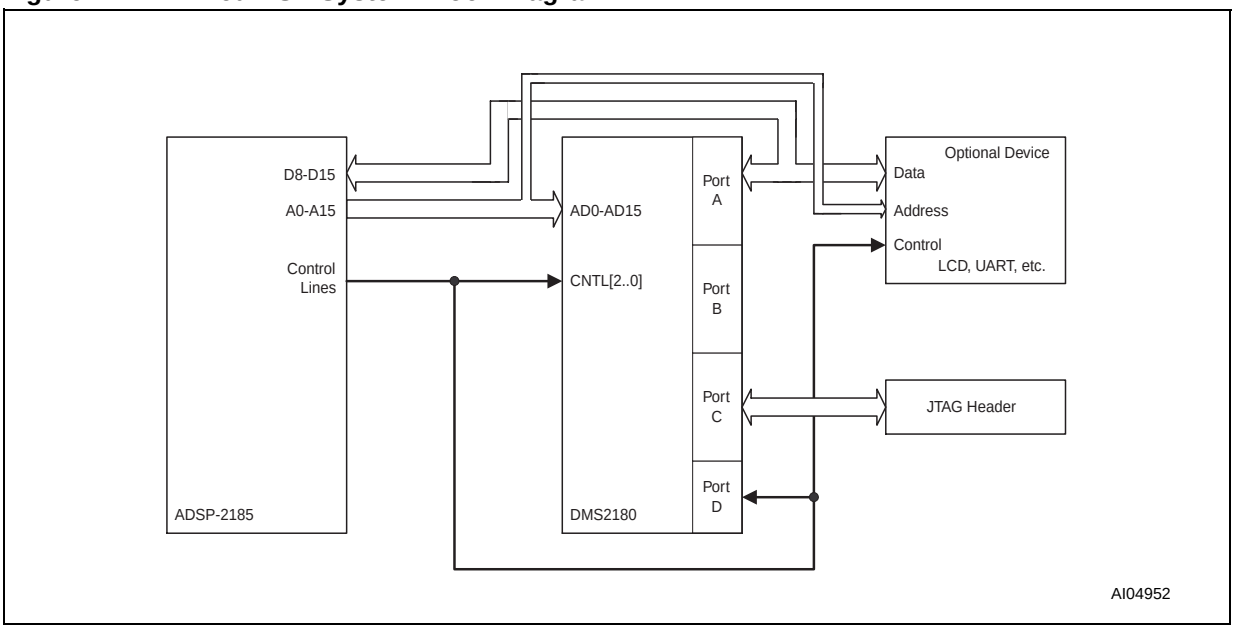
The ADSP-2185 contains the following:

- An on-chip 8-bit Automatic Boot Loader through DMA interface or memory port
- 80 KBytes RAM configures as:
- 16 KWords Program Memory RAM (24-bit)
- 16 KWords Data Memory RAM (16-bit)
- Dual-purpose Program Memory for both instructions and data storage.

The low-cost DSM2180F3 is selected for this design to take advantage of the ADSP-2185 resident boot loader, using its Flash memory to store the downloadable ADSP-2185 program code.

Figure 2 is a basic block diagram that shows the implementation of a basic system using the DSM2180F3/ADSP-2185 two-chip combination. All glue logic, Flash memory, bus interface logic, I/O, chip selects, and PLDs are contained in the DSM chip.

Figure 2. Minimized DSP System Block Diagram



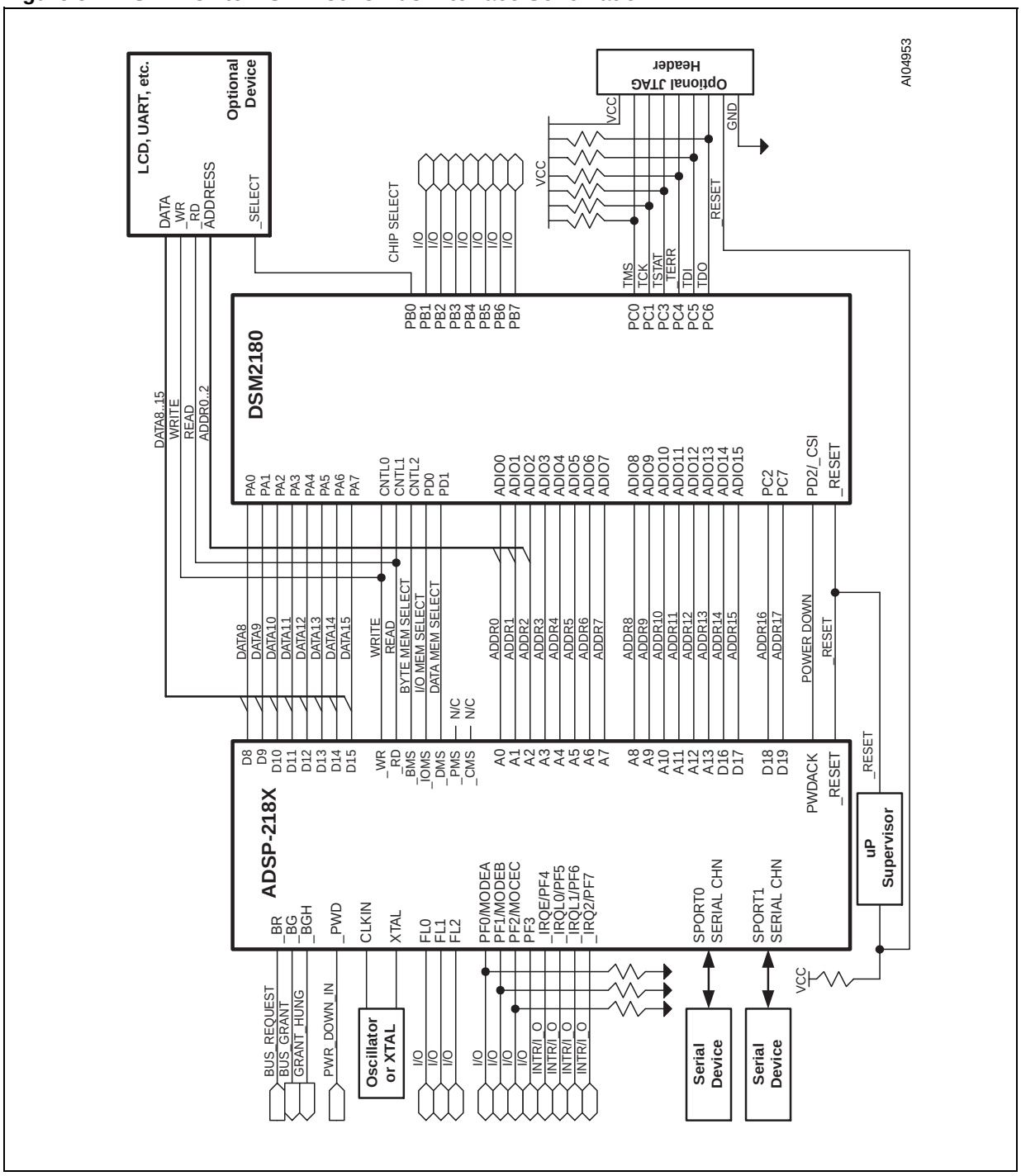
DSM2180F3 Bus Interface

When an ADSP218x is selected in PSDsoft Express (see Section 6), the bus interface is pre-configured so there is no chance to make a configuration mistake. Table 2 lists the bus interface signals from the ADSP-2185 used to access the Flash memory, PLD logic, and I/O inside the DSM2180F3. These signals are automatically configured when the ADSP-218X is selected.

Table 1. ADSP-2185 / DSM2180F3 Bus Interface Pin Functions

ADSP-2185 Pin Functions	DSM2180F3 Pin Functions	Pin Description
A [15:0]	ADIO [15:0]	External Address Bus addresses all external memory - Program, Data and I/O.
D [7:0]	N.C.	8 high byte bi-directional external Data bus lines.
D [15:8]	Port A:PA [7:0]	8 low byte bi-directional external Data bus lines.Port A is used as the 8-bit Data bus into the DSM2180F3.
/WR	CNTL0	Write signal is used to access external memory during memory write cycles.
/RD	CNTL1	Read signal is used to access external memory during memory read cycles.
/BMS	CNTL2	Byte Memory Select signal is used for external 8-bit data memory accesses.
/RESET	_RESET	System reset input

Figure 3. ADSP-218x to DSM2180F3 Bus Interface Schematic



ADSP-218X to DSM2180F3 Schematic

Figure 3 shows an example schematic diagram for an ADSP-218x to DSM2180F3 design. While Table 1 shows the required connections for every design, the schematic shows additional signals and functions that would be typical of many designs. Specifically, the following signals have been added:

Table 2. ADSP-2185 / DSM2180F3 Optional Signals Used

ADSP-2185 Pin Functions	DSM2180F3 Pin Functions	Pin Description
/IOMS	PD0	I/O Memory Select signal
/DSM	PD1	Data Memory Select signal
D18	PC2	Address bit 16
D19	PC7	Address bit 17
PWDACK	PD2/_CSI	Power down chip select signal
N/A	PB2	Chip Select for external device, such as LCD, UART, etc.

Note: The schematic also shows basic ADSP-218x connections, such as the system reset input and the DSM2180F3 shows additional optional connections, such as I/O and JTAG.

DEFINE THE ADSP-2185 INTERFACE IN PSDSOFT EXPRESS

Highlights of design entry will be given here. Please refer to the PSDsoft Express User Manual for a thorough coverage of all the features of PSDsoft Express. This section is meant to show you just the essentials to get you going. Here are the steps when using a template:

Invoke PSDsoft Express and Open a New Project

- Start PSDsoft Express.
- Create a new project.
- Select your project folder and name the project (in this example, name the project “DSM2180” in the folder PSDsoft\my_project).

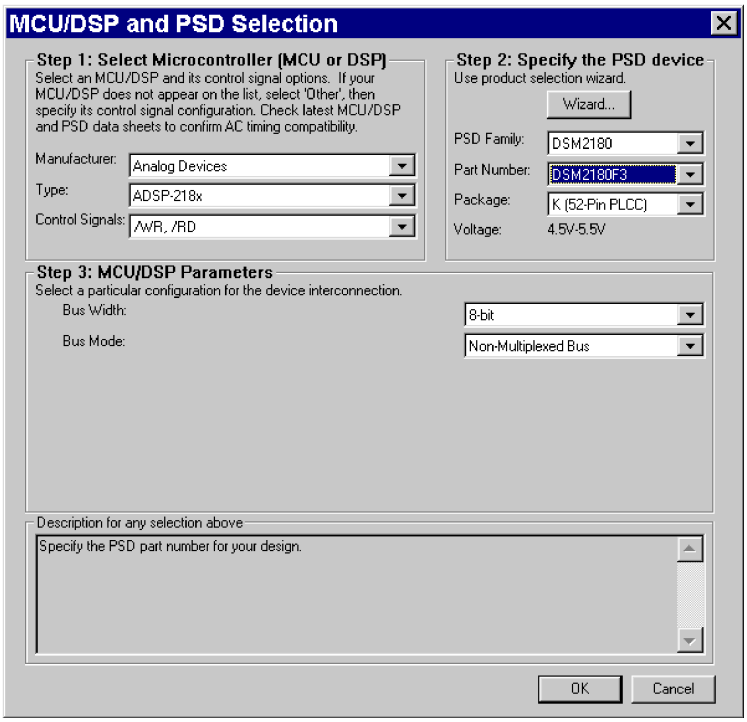
The associated dialog box is shown graphically in Figure 4.

MCU/DSP and PSD Selection

When you click **OK** in the “New Project” window, the “MCU and PSD Selection” screen appears. When you see this screen, make the following selections:

- Select Analog Devices for the manufacturer and ADSP 218x for the type
- The control signals are selected for you.
- Select the DSM2180 for the Family, the DSM2180F3 for the part and the K package.
- The MCU/DSP parameters are set for you. Click **OK**.

Figure 4. PSDsoft Express Define DSM and MCU/DSP


MCU/DSP and PSD Selection
Step 1: Select Microcontroller (MCU or DSP)
Select an MCU/DSP and its control signal options. If your MCU/DSP does not appear on the list, select 'Other', then specify its control signal configuration. Check latest MCU/DSP and PSD data sheets to confirm AC timing compatibility.
Manufacturer: Analog Devices
Type: ADSP-218x
Control Signals: /WR, /RD
Step 2: Specify the PSD device
Use product selection wizard.
Wizard...
PSD Family: DSM2180
Part Number: DSM2180F3
Package: K (52-Pin PLCC)
Voltage: 4.5V-5.5V
Step 3: MCU/DSP Parameters
Select a particular configuration for the device interconnection.
Bus Width: 8-bit
Bus Mode: Non-Multiplexed Bus
Description for any selection above
Specify the PSD part number for your design.
OK
Cancel

Now you have your project established based on a DSM2180F3 and an ADSP-2185.

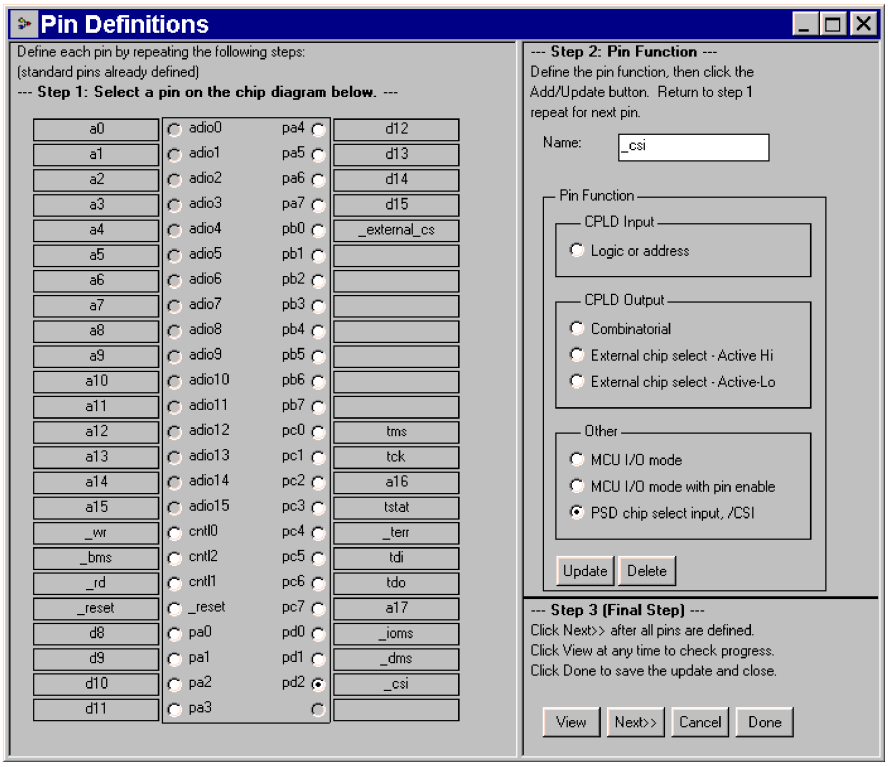
When the “Design Parameters” screen appears, choose “Use example template selection” and click OK to be taken to the “MCU Template Selection” screen.

Now choose “Application Note 076, DSP loader” and click Generate. This will automatically setup the extra pins described in Table 2 and the memory map described in the next section

Pin Definitions

Your pin definitions should match Figure 5 and are defined according to the schematic shown in Figure 3. On this screen, you can add or update pin functionality as desired. When you are finished, clicking **Next>>** will take you to the “Design Assistant” screen, which will be covered in the next section.

Figure 5. DSM2180F3 Pin Definitions


Pin Definitions
Define each pin by repeating the following steps:
(standard pins already defined)
--- Step 1: Select a pin on the chip diagram below. ---
--- Step 2: Pin Function ---
Define the pin function, then click the Add/Update button. Return to step 1 repeat for next pin.
Name: _csi
Pin Function
CPLD Input
Logic or address
CPLD Output
Combinatorial
External chip select - Active Hi
External chip select - Active-Lo
Other
MCU I/O mode
MCU I/O mode with pin enable
PSD chip select input, /CSI
Update
Delete
--- Step 3 (Final Step) ---
Click Next>> after all pins are defined.
Click View at any time to check progress.
Click Done to save the update and close.
View
Next>>
Cancel
Done

Note: There are detailed instructions on how to use this screen and other screens in the PSDsoft Express User Manual.

ADSP-2185 BOOT LOADER

The ADSP-2185 has two mechanisms to allow automatic loading of the internal program memory after reset which are BDMA boot or IDMA boot. Either mode can be used with the DSM2180F3, however, this application note uses BDMA booting. The method for booting is controlled by the Mode A, B and C configuration bits. See the ADSP-2185 data sheet for details on the boot methods and Mode pins.

ADSP-2185 MEMORY MAP

The ADSP-2185 uses a modified Harvard architecture with up to four independent memory spaces (I/O, Data, Program, and Combined). It contains 16 KWords (x16) of on-chip Data Memory (DM) Ram and 16 KWords (x24) of on-chip Program Memory (PM) RAM. See the ADSP-2185 data sheet from Analog Devices for details on the memory architecture.

Figure 6 shows one possible memory map. The nomenclature fs0.fs7 are individual 16 KByte Flash memory segment designators within the DSM and “csiop” designates the DSM control register block. For this memory map, the DSP should be set to run in Full Memory Mode. Memory contents of the DSM device may lie in one or more of three different DSP address spaces; I/O space (with limited address lines), byte DMA space, and/or External Data-overlay Memory Space (DMS). Since the DSM device is a byte-wide memory, awareness of the natural x16 and x24 nature of DM and PM respectively is important. The designer may easily specify memory mapping in a point-and-click software environment using PSDsoft Express™. Since the memory mapping is implemented with the DPLD and the Page Register, many possibilities exist.

The memory map is organized to work within the restrictions of the ADSP-2185 Boot Loader (discussed in the previous section) and to utilize the entire Flash memory and show the paging features of the DSM2180F3.

Figure 6. ADSP-2185/DSM2180F3 Memory Map

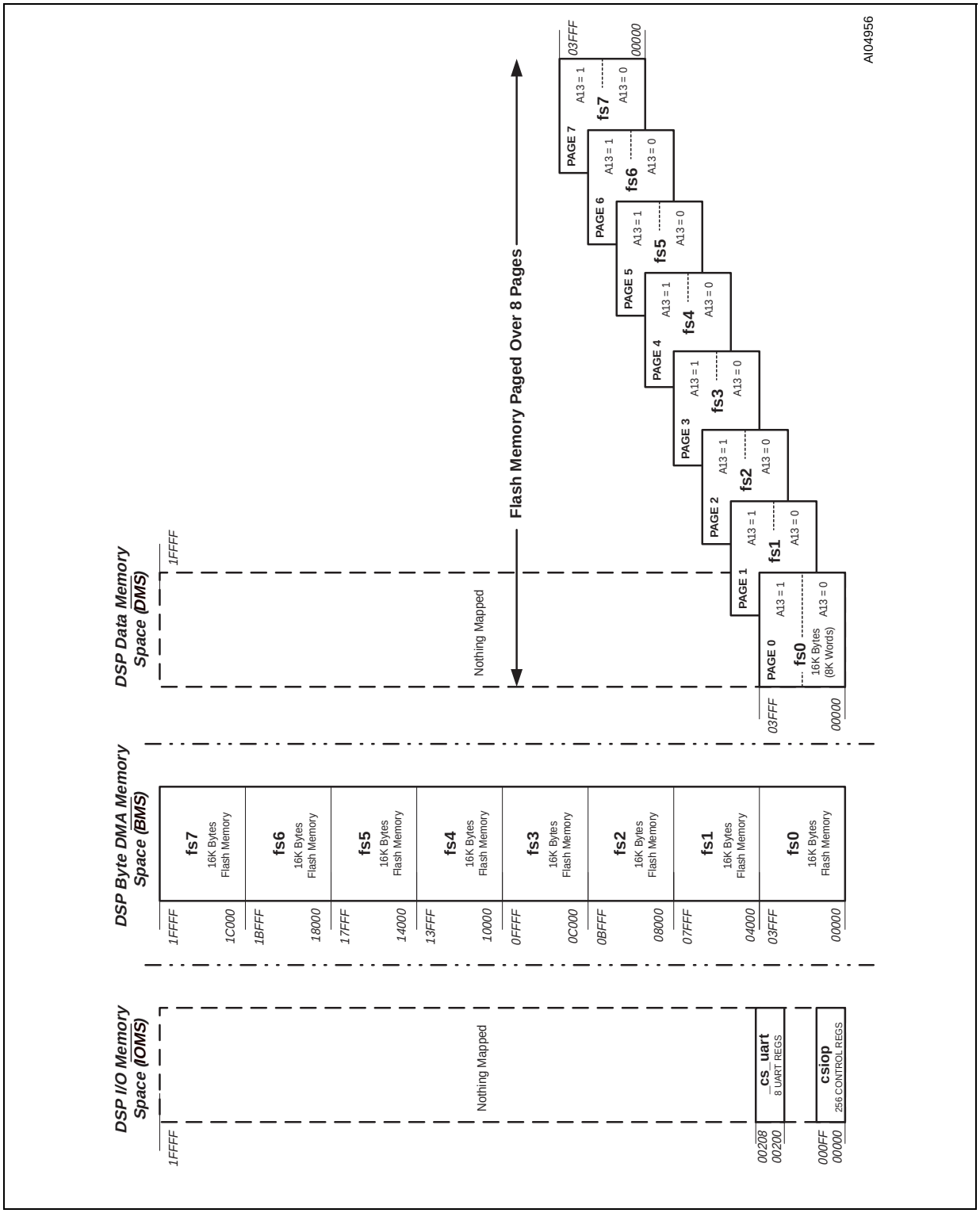


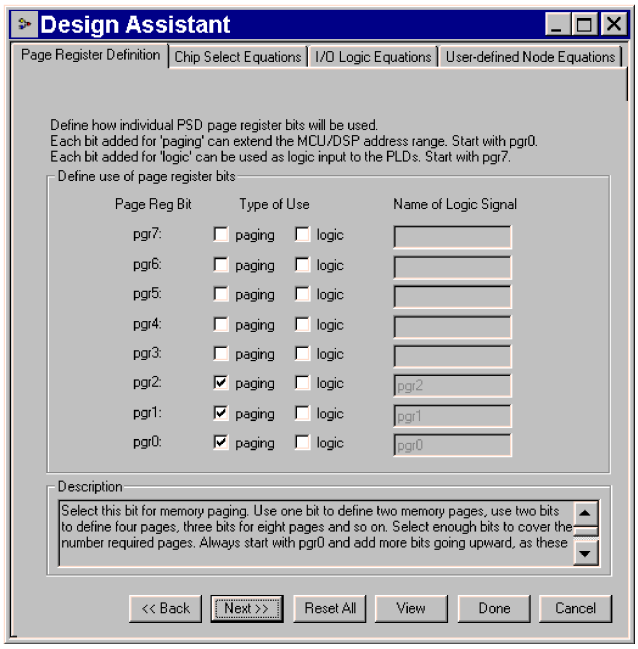
Figure 6 shows a typical memory map with the following attributes:

- I/O Address Space. The 256 byte locations for DSM control registers (csiop) reside in DSP I/O address space, selected by the DSP IOMS signal. Since DSP I/O accesses are 16 bits, not 8 bits, the upper byte of a 16-bit DSP I/O access must be ignored.
- Byte DMA Address Space. The DSP may boot-load or fetch overlay bytes from 128 KBytes of Flash memory using the DSP BDMA channel. The DSP may also write to Flash memory using the Byte DMA channel. DSM Flash memory is accessed in 128 KB continuous byte address locations through the BDMA channel and is selected whenever the DSP BMS signal is active. Flash memory in the DSM device must be un-locked and written by the DSP one byte at a time, checking status after each write (typical Flash memory programming algorithm).
- Data Overlay Memory Address Space. All 128 KBytes of Flash memory also reside in DSP External Data-overlay Memory Space, selected by DMS, allowing more efficient byte writes to Flash memory. The DSP uses its external data overlay window of 8 KB locations to access external memory as data. The DSP doubles the size of this window to 16 KB locations by manipulating its A13 address line using its DMOVLAY register (See the ADSP-2185 data sheet for details). Since all 128 KBytes of Flash memory must be accessed through a window of only 16 KB locations, the DSP uses the Page Register inside the DSM device to page through 8 pages of 16 KBytes, as shown in Figure 6. Since DSP Data accesses are by 16 bits, not 8 bits, the upper byte of a 16-bit DSP Data access must be ignored.

Define the Memory Map in PSDsoft Express

The template's memory map is setup according to Figure 6. First, note how the Page Register is setup, shown in Figure 7.

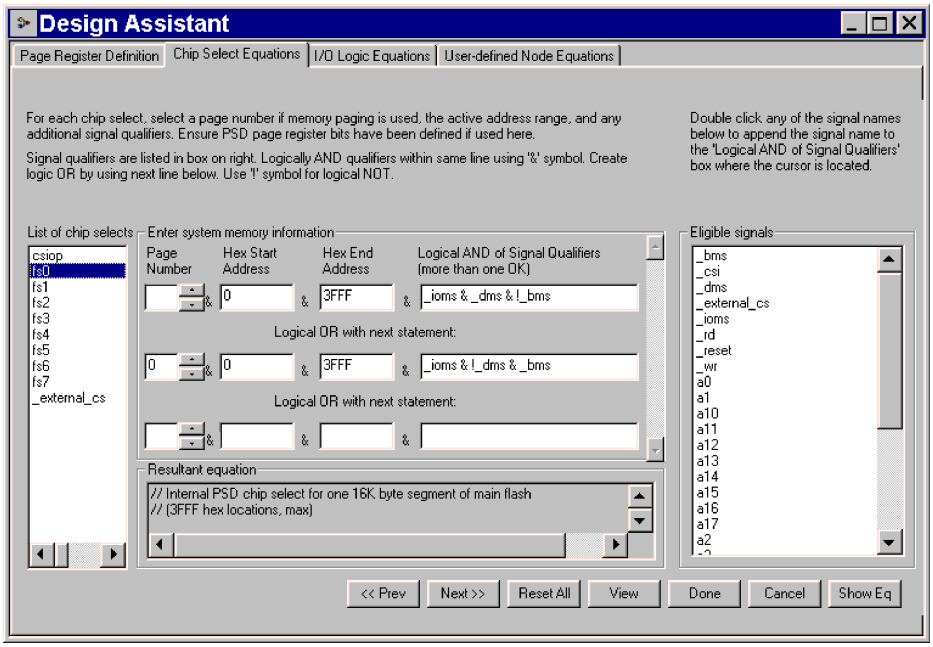
Figure 7. DSM2180F3 Page Register Setup


Design Assistant
Page Register Definition
Chip Select Equations
I/O Logic Equations
User-defined Node Equations
Define how individual PSD page register bits will be used.
Each bit added for 'paging' can extend the MCU/DSP address range. Start with pgr0.
Each bit added for 'logic' can be used as logic input to the PLDs. Start with pgr7.
Define use of page register bits
Page Reg Bit
Type of Use
Name of Logic Signal
pgr7: paging logic
pgr6: paging logic
pgr5: paging logic
pgr4: paging logic
pgr3: paging logic
pgr2: paging logic pgr2
pgr1: paging logic pgr1
pgr0: paging logic pgr0
Description
Select this bit for memory paging. Use one bit to define two memory pages, use two bits to define four pages, three bits for eight pages and so on. Select enough bits to cover the number required pages. Always start with pgr0 and add more bits going upward, as these
<< Back
Next >>
Reset All
View
Done
Cancel

The memory map is organized to work within the restrictions of the ADSP-2185 Boot Loader and to utilize the entire Flash memory and show the paging features of the DSM2180F3.

The three paging bits will provide 2^3 = 8 pages. Click **Next** to see the Chip Selection Equations screen, shown in Figure 8.

Figure 8. DSM2180F3 Chip Select Equations



If you click on each of the chip select signals in the list on the list, you will see that they have all been defined according to the memory map in Figure 6. Note that all the chip-select equations are listed in the Appendix.

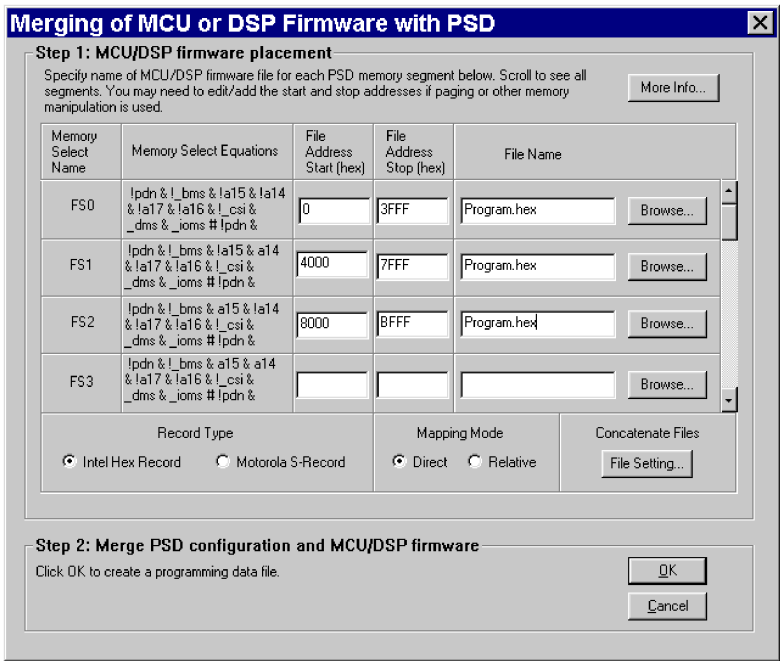
The I/O Logic Equations and User-defined Equations tabs are used to implement general-purpose combinatorial and sequential logic. These topics are covered in more detail in the PSDsoft Express User Manual: http://www.psdst.com/html/psdsoft_exp.htm. When you are ready to see how the DSP firmware can be loaded into the DSM via the programming data file (.obj), click **Done**.

Loading the ADSP Firmware into the DSM

Now that you have completed the definitions of the DSM's internal and external signals, it is time to load the ADSP firmware into the DSM. To accomplish this, take the following steps:

- Click the Fit Design to Silicon button in the PSDsoft Express design flow. Since this is a template, the design should fit without errors if you have not modified the design. If you do get an error, you will need to fix it before moving on.
- Take note of the Generate C Code button. It is used to generate flash routines that can be pasted into your C Code before compiling and linking. This is not required for the presented design.
- Click the Merge MCU/DSP firmware with PSD button. This step is where the DSM configuration/mem map are merged with the output of the compiler/linker tools chain. Upon invocation, you will get a warning that basically says, since paging was used in the design, the software is not sure how to fill in the file start and stop addresses and you will have to do it manually. Figure 9 shows an example of how this might be filled in and assumes that a file called "Program.hex" has been previously generated, taking up the first three DSM flash segments. Note the scroll bar on the right to access memory beyond fs3. Click **OK** to generate the programming data file (.obj) that will be used to program the device. That's it; you are now ready to program the device. For more information on how to program the DSM through the JTAG port or a conventional programmer, consult the PSDsoft Express User Manual: http://www.psdst.com/html/psdsoft_exp.htm.

Figure 9. Merging of DSP Firmware with DSM Memory Map


Merging of MCU or DSP Firmware with PSD
Step 1: MCU/DSP firmware placement
Specify name of MCU/DSP firmware file for each PSD memory segment below. Scroll to see all segments. You may need to edit/add the start and stop addresses if paging or other memory manipulation is used.
More Info...
Memory Select Name
Memory Select Equations
File Address Start (hex)
File Address Stop (hex)
File Name
FS0
!pdn & !_bms & !a15 & !a14 & !a17 & !a16 & !_csi & _dms & _ioms # !pdn &
0
3FFF
Program.hex
Browse...
FS1
!pdn & !_bms & !a15 & a14 & !a17 & !a16 & !_csi & _dms & _ioms # !pdn &
4000
7FFF
Program.hex
Browse...
FS2
!pdn & !_bms & a15 & !a14 & !a17 & !a16 & !_csi & _dms & _ioms # !pdn &
8000
BFFF
Program.hex
Browse...
FS3
!pdn & !_bms & a15 & a14 & !a17 & !a16 & !_csi & _dms & _ioms # !pdn &
Browse...
Record Type
Intel Hex Record
Motorola S-Record
Mapping Mode
Direct
Relative
Concatenate Files
File Setting...
Step 2: Merge PSD configuration and MCU/DSP firmware
Click OK to create a programming data file.
OK
Cancel

PROGRAMMING THE DSM2180F3 IN-CIRCUIT USING THE JTAG INTERFACE

The ability to initially program a new system board with a blank Flash memory soldered directly to it has solved many manufacturing logistics problems: no sockets or individual labels are required; inventory of non-volatile program memory chips is reduced to one package; the PLD is programmed at the same time as the memory chip: one system board can be built and inventoried; and options can be programmed into the Flash memory at board level testing.

Port C I/O lines are used to interface to the standard JTAG signals - TMS, TCK, TDI and TDO. TSTAT and TERR are optional JTAG-ISP extensions that can be monitored to decrease the programming time of the DSM2180F3. The DSM configuration, PLD logic, and Flash memory can all be programmed through the JTAG port.

Port C JTAG pins can also be multiplexed with other signals, such that the signals are used to program the DSM while the DSP is held in reset and as general I/O during normal DSP operation. The cost of JTAG muxing is a single pin on the DSM to control the state of this mux. This option frees up the JTAG pins for I/O functions after JTAG programming is complete. For more information on how the JTAG port can be multiplexed, see Application Note *AN1153* and the PSDsoft Express User Manual at: http://www.ps-dst.com/html/psdsoft_exp.htm. Also note that the DK-2180 development board multiplexes the JTAG signals and has a slightly different pin configuration.

SUMMARY

As DSPs continue to proliferate into markets such as communications, industrial, medical, signal conditioning, and hand held test equipment, the DSM2180F3 and DSP form an ideal 2-chip solution with on-chip PLD and I/O lines that are individually configured to perform any function required by the system design. Using the DSM2180F3 as an 8-bit boot loader in both high speed and low speed systems is an ideal and rapid design alternative to a discrete solution. Inexpensive slower memory and PLDs integrated in the DSM2180F3 now become both cost and performance effective.

Several features of the DSM2180F3 were used to expand the functionality of the ADSP-2185, including:

- In-System Programmable Flash memory.
- JTAG-ISP to simplify manufacturing.
- Expanded I/O.
- Interfacing to external devices was easily accomplished by generating the required control signals in the internal programmable PLD.
- A quick and easy design prototype using PSDsoft Express.

These changes have added to both the versatility and performance of the ADSP-2185.

APPENDIX

The Appendix contains the PSDsoft Express Design Assistant Summary listing all logic equations to show how the DSM2180F3 is configured for the ADSP-2185 interface in order to implement the example in this Application Note. Application Note *AN1356* presents a step-by-step illustration of how to configure the Flash DSM Family. Although *AN1356* uses the 16-bit Flash PSD4235G2 in the example, the software and procedure is the same for the 8-bit DSM2180F3.

```
******************************************************************************
                         PSDsoft Express Version 7.10
                         Summary of Design Assistant
******************************************************************************
PROJECT    : AN076                          DATE : 05/21/2001
DEVICE     : DSM2180F3                      TIME : 13:05:59
MCU/DSP    : ADSP-218x
******************************************************************************

Pin Definitions:
================

Pin          Signal       Pin
Name         Name         Type
------------ ------------ ------------
adio0        a0           Address line
adio1        a1           Address line
adio2        a2           Address line
adio3        a3           Address line
adio4        a4           Address line
adio5        a5           Address line
adio6        a6           Address line
adio7        a7           Address line
adio8        a8           Address line
adio9        a9           Address line
adio10       a10          Address line
adio11       a11          Address line
adio12       a12          Address line
```

```
adio13      a13         Address line
adio14      a14         Address line
adio15      a15         Address line
cntl0       _wr         DSP bus control signal
cntl2       _bms        DSP bus control signal
cntl1       _rd         DSP bus control signal
reset       _reset      RESET input
pa0         d8          Data line
pa1         d9          Data line
pa2         d10         Data line
pa3         d11         Data line
pa4         d12         Data line
pa5         d13         Data line
pa6         d14         Data line
pa7         d15         Data line
pb0         _cs_uart    External chip select - Active-Lo
pc0         tms         Dedicated JTAG - TMS
pc1         tck         Dedicated JTAG - TCK
pc2         a16         Logic or address
pc3         tstat       Dedicated JTAG - TSTAT
pc4         _terr       Dedicated JTAG - /TERR
pc5         tdi         Dedicated JTAG - TDI
pc6         tdo         Dedicated JTAG - TDO
pc7         a17         Logic or address
pd0         _ioms       Logic or address
pd1         _dms        Logic or address
pd2         _csi        PSD chip select input, /CSI

User defined nodes:
==================

None defined

Page Register settings:
=======================
pgr0 is used for paging
pgr1 is used for paging
pgr2 is used for paging
pgr3 is not used
pgr4 is not used
pgr5 is not used
pgr6 is not used
pgr7 is not used

Equations:
==========

csiop = ((address >= ^h0000) & (address <= ^h00FF) & (!_ioms & _dms & _bms));
fs0 = ((address >= ^h0000) & (address <= ^h3FFF) & (_ioms & _dms & !_bms))
     # ((page == 0) & (address >= ^h0000) & (address <= ^h3FFF) & (_ioms & !_dms & _bms));
fs1 = ((address >= ^h4000) & (address <= ^h7FFF) & (_ioms & _dms & !_bms))
     # ((page == 1) & (address >= ^h0000) & (address <= ^h3FFF) & (_ioms & !_dms & _bms));
fs2 = ((address >= ^h8000) & (address <= ^hBFFF) & (_ioms & _dms & !_bms))
     # ((page == 2) & (address >= ^h0000) & (address <= ^h3FFF) & (_ioms & !_dms & _bms));
fs3 = ((address >= ^hC000) & (address <= ^hFFFF) & (_ioms & _dms & !_bms))
     # ((page == 3) & (address >= ^h0000) & (address <= ^h3FFF) & (_ioms & !_dms & _bms));
fs4 = ((address >= ^h10000) & (address <= ^h13FFF) & (_ioms & _dms & !_bms))
     # ((page == 4) & (address >= ^h0000) & (address <= ^h3FFF) & (_ioms & !_dms & _bms));
fs5 = ((address >= ^h14000) & (address <= ^h17FFF) & (_ioms & _dms & !_bms))
```

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    # ((page == 5) & (address >= ^h0000) & (address <= ^h3FFF) & (_ioms & !_dms & _bms));
fs6 = ((address >= ^h18000) & (address <= ^h1BFFF) & (_ioms & _dms & !_bms))
    # ((page == 6) & (address >= ^h0000) & (address <= ^h3FFF) & (_ioms & !_dms & _bms));
fs7 = ((address >= ^h1C000) & (address <= ^h1FFFF) & (_ioms & _dms & !_bms))
    # ((page == 7) & (address >= ^h0000) & (address <= ^h3FFF) & (_ioms & !_dms & _bms));
!_external_cs = ((address >= ^h0200) & (address <= ^h0207) & (!_ioms & _dms & _bms));
```

Table 3. Document Revision History

Date	Rev.	Description of Revision
21-Jun-2001	1.0	Document written

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